

Class-F Amplifier Loading Networks: A Unified Design Approach

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Abstract

A method is shown which greatly simplifies the design of third-order loading networks for Class-F switching amplifiers. The goal of the method is to determine the approximate component values for interstage and final amplifier loading networks that present the proper load conditions at the primary frequency f_0 and its third harmonic $3f_0$, while at the same time introducing a low impedance to ground at the second harmonic frequency $2f_0$. Design procedures and equations are presented for one class of final amplifier and three classes of interstage loading networks.

Introduction

Class-F amplifiers have enjoyed wide-spread application in recent years, due to an overwhelming need to improve transmitter power amplifier efficiency in both portable and fixed-base communications, as well as commercial FM broadcasting. Since the power amplifier of a transmitter consumes most of the power, its efficiency determines the overall power and heat dissipation requirements. The process of improving the efficiency of high-power amplifiers has been known for a considerable amount of time¹, but saw little application until the wide-spread use of FM for mobile communications and commercial broadcasting in the 1950's, its reintroduction in the professional literature², and subsequent patenting³.

Since that time, much has been written concerning the principles and applications of Class-F

power amplifiers⁴⁻⁸, and the requirements for satisfying the multiple simultaneous loading requirements in the design process has prompted the need for deriving a systematic procedure for designing interstage and final amplifier loading networks in a way that does not impact manufacturing costs.

Briefly, a Class-F amplifier derives its improved efficiency by using a multiple-resonator loading network to control the harmonic content of the drain voltage and/or drain current waveforms.⁹ This paper will address the design of loading networks for one of the basic circuit forms known as third-harmonic peaking, the voltage waveforms for which are shown in Figure 1 and the representative loading circuits are shown in the appendix.

Referring to Figure 1, the drain voltage for third-order peaking consists of the sum of the fundamental signal voltage at frequency f_0 and its third harmonic voltage at frequency $3f_0$. Note that the result of this summation is that the peak amplitude of the voltage waveform is decreased at 90 and

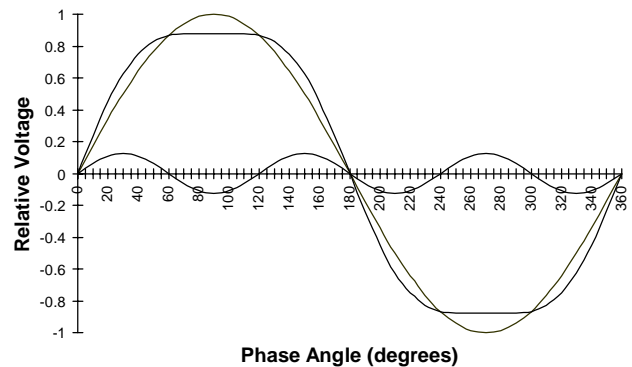


Figure 1 - Third-Order Waveforms

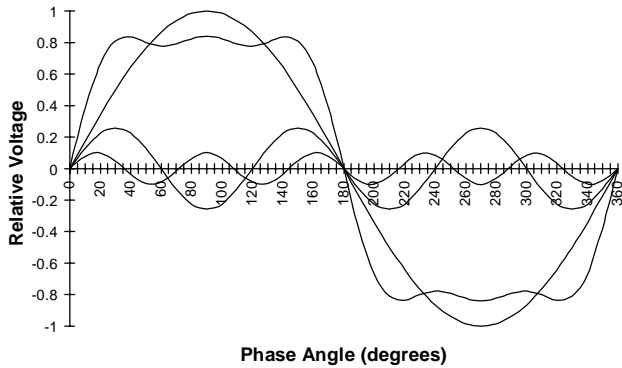


Figure 2 - Fifth-Order Waveforms

270 degrees. A similar voltage waveform for fifth-harmonic peaking is shown in Figure 2. In general, odd-harmonic peaking circuits above this level are rarely, if ever, seen and even the fifth-order realizations deliver less than a 10% improvement in amplifier power efficiency over that of the third-order circuits.

The presence of second harmonic and higher even-order harmonic voltages will cause this waveform to reach saturation or cutoff earlier than desired, resulting in a rapid loss of efficiency. It would therefore be desirable to design loading networks in such a way as to achieve the necessary load impedance and matching requirements, but without introducing excessive complexity, component count, alignment, or other factors that would have a negative impact on manufacturing costs.

Final Amplifier Loading Network

A schematic diagram of a loading network commonly seen in final amplifier stages is shown in the appendix. Here, the parallel network L_1/C_1 is resonant at the fundamental frequency f_0 , while the parallel-resonant idler network L_2/C_2 is resonant at the third harmonic $3f_0$. In general, the series capacitor C_3 is considered to be nothing more than a DC blocking capacitor, but instead will now be considered as part of the overall loading network. At the fundamental frequency f_0 , the third-harmonic idler L_2/C_2 represents a small inductance between the drain and the load which can be tuned

out by adjusting the value of C_3 to improve coupling to the load. In addition, at the second harmonic $2f_0$ the still inductive third-harmonic idler is in series with the now capacitive fundamental tank L_1/C_1 and the DC blocking capacitance C_3 . By proper selection of these five reactive elements, a loading network can be derived that will satisfy all three requirements simultaneously.

The design procedure begins with the selection of capacitor C_1 , which is determined by the load resistance R_L , the centre frequency ω_0 , and the desired bandwidth BW. The values for L_1 , L_2 , C_2 , and C_3 are then determined in order as shown.

Interstage Loading Networks

Three networks suitable for interstage loading are shown in the appendix. In the first of these, referred to as Type 1, the parallel network L_1/C_1 is resonant at the fundamental frequency f_0 and the parallel network L_2/C_2 is resonant at the third harmonic $3f_0$. At the second harmonic $2f_0$, the fundamental tank L_1/C_1 is capacitive, while the third harmonic idler L_2/C_2 is inductive. By proper selection of these four components, these two reactances can be made series resonant at the second harmonic, thereby fulfilling all three desired characteristics of the loading network simultaneously. The design procedure begins with the arbitrary selection of C_1 , as the process of determining the value empirically is unnecessarily tedious. The remaining component values are then determined by way of the equations as shown.

A difficulty with the Type 1 network arises when trying to incorporate the reactances of the amplifier device and the subsequent load device. The Type 2 interstage network (see the appendix) overcomes this difficulty by having its fundamental resonant capacitor C_1 in shunt across the entire network. The sum of the apparent inductance of the parallel resonant tank L_2/C_2 and inductor L_1 create a resonance at the fundamental frequency f_0 . The L_2/C_2 tank is actually resonant below $2f_0$, and the subsequent apparent series capacitance of this

tank in series with L_1 creates a low-impedance series resonance at $2f_0$. At $3f_0$, the apparent inductance of this leg creates a parallel resonance with C_1 .

The design procedure is more straightforward than with the previous Type 1 network, and the value of C_1 is derived from the load resistance R_L , the centre frequency ω_0 , and the desired bandwidth BW. The subsequent values for L_1 , C_2 , and L_2 are derived as shown.

Tuning this network is not as straightforward as with Type 1, and matching to the load device by splitting capacitor C_1 may result in a match having a higher Q than would be desirable.

The Type 3 interstage network (see the appendix) retains the desirable characteristics of Type 2, while at the same time providing a means for matching to the load device without increasing the matching Q. Here, C_2 and L_2 are series resonant at the second harmonic $2f_0$. At f_0 this network is capacitive, and together with L_1 and C_1 creates a parallel resonant tank. At $3f_0$ the L_2/C_2 leg is inductive, and again with L_1 and C_1 creates a third-harmonic parallel resonant tank. The active device reactances can now be easily incorporated into either L_1 or C_1 , and a low-Q load match is readily accomplished by simply tapping L_1 . Component values are determined in the same manner as with the Type 2 network.

Conclusions

The component values derived here are approximations, as the parasitic reactances (normally capacitive) of the active devices will alter the resonances of the networks. It is best to use these approximations as a starting point, referring the design to a computer optimization routine prior to committing to hardware.

In general, the best bandwidth is derived by designing the networks in such a manner as to cause the Q of the two resonant tanks and the Q of the second harmonic null to be nearly equal.

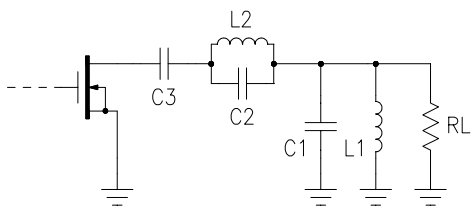
These design procedures have been used, in

part in the design of VHF Class-F power amplifiers achieving peak power drain efficiencies of over 95%, and an 80% drain efficiency bandwidth of over 8%. A similar set design procedures have been derived for fifth-order peaking networks.

References

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APPENDIX



THIRD-ORDER FINAL NETWORK

First, choose C_1 :

$$C_1 = a / [(1 - a^2) \omega_0 R_L]$$

where

$$a = (\omega_0 - p BW) / \omega_0$$

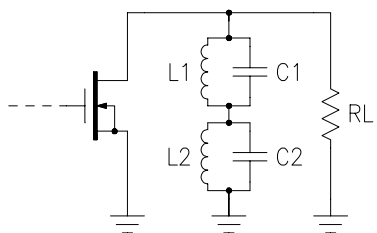
Now,

$$L_1 = 1 / (\omega_0^2 C_1)$$

$$L_2 = 160 L_1 R_L^2 / \{ 81 [(3 R_L)^2 + (2 \omega_0 L_1)^2] \}$$

$$C_2 = 1 / (9 \omega_0^2 L_2)$$

$$C_3 = 8 C_2$$



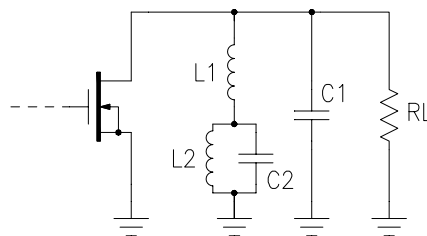
Third-Order Interstage Network (Type 1)

First, choose C_1 arbitrarily. Now,

$$L_1 = 1 / (\omega_0^2 C_1)$$

$$C_2 = 3 C_1 / 5$$

$$L_2 = 5 L_1 / 27$$



Third-Order Interstage Network (Type 2)

First, choose C_1 :

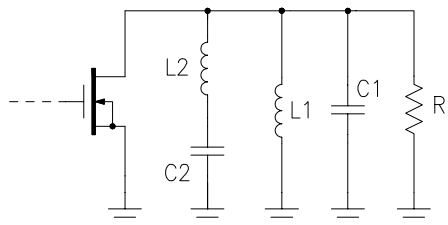
$$C_1 = 1 / [(\omega_0 + p BW) R_L]$$

Now,

$$L_1 = 2 / [3 (\omega_0^2 C_1)]$$

$$C_2 = 5 C_1 / 12$$

$$L_2 = 3 L_1 / 5$$



Third-Order Interstage Network (Type 3)

First, choose C_1 :

$$C_1 = 1 / [(\omega_0 + p BW) R_L]$$

Now,

$$L_1 = 4 / [9 (\omega_0^2 C_1)]$$

$$C_2 = 15 C_1 / 16$$

$$L_2 = 9 L_1 / 15$$